UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,348	01/15/2004	Edwin Frank Barry	800.0139	5315

27997 7590 07/06/2004

PRIEST & GOLDSTEIN PLLC
5015 SOUTHPARK DRIVE
SUITE 230
DURHAM, NC 27713-7736

EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,348	BARRY ET AL.	
	Examiner	Art Unit	
	Alan S Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-8,13-15 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-8,13-15 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 14 is objected to because of the following informalities: line 3 in claim 14 contains a misspelling of the word port. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 6-8, 13-15 and 17-22 are rejected under 35 U.S.C. 102(e) as being anticipated by No. 6,055,619 to North et al. (hereafter North).

3. As per claim 6, North discloses a VIM DMA apparatus (Fig. 1) comprising: a partitioned VIM having a separate VIM section per VLIW slot function unit (Fig. 1, element 101); a DMA interface (Fig. 2A, element 208), a DMA VLIW line buffer (Fig. 2A, element 208); and a VIM load controller for separately controlling the loading of each separate VIM section (Column 8, lines 27-65 and column 10, lines 1-16).

4. As per claim 7, North discloses a claim 6, wherein each separate VIM section has two ports allowing simultaneous read and write accesses (Fig. 1, element 101 had input and output ports).

5. As per claim 8, North discloses claim 6 wherein said line buffer (Fig. 2A, element 208) receives and temporarily stores a data packet comprising a load/modify VLIW memory address

(LV2) instruction and a plurality of short instruction words (SlWs) constituting a specified functional VIM portion to be loaded at an address specified in the LV2 instruction (Column 8, lines 55-65).

6. As per claim 13, North discloses a type of method for providing VIM DMA, said method comprising the steps of: storing a DMA VLIW line buffer (Fig. 2A, element 208); utilizing a VIM load controller for separately controlling the loading of each separate VIM section in a partitioned VIM having a separate VIM section per VLIW slot function unit (Fig. 1, element 104); and selectively routing the appropriate portions of said VLIW from said line buffer to said separate VIM sections on a DMA interface (2A, element 208).

7. As per claim 14, North discloses claim 13, wherein each separate VIM section has two ports allowing simultaneous read and write accesses, and the method further comprises the step of separately providing each of the two ports for each separate VIM section its open address and read or write control signals (Fig. 1, element 101 has own input and output lines).

8. As per claim 15, North discloses claim 13 further comprising the step of receiving and temporarily storing in said line buffer (Fig. 2A, element 202) a plurality of data packets comprising a load/modify VLIW memory address (LV2) instruction and a plurality of short instruction words (SIWs) constituting a specified functional VIM portion to be loaded at an address specified in the LV2 instruction (Fig. 1).

9. As per claim 17, North discloses a VIM DMA apparatus comprising: a plurality of function execution units (Fig. 2A), each function execution unit performing a distinct operation (e.g., processor performs calculations, DMA interfaces PCI, etc.); a VIM having a plurality of VIM sections (Fig. 1, element 101), each VIM section storing instructions corresponding to each

functional execution limit, each VIM section associated with a functional execution unit (operates with the processor core, within the processor, there are a plurality of functional execution units, Fig. 1), each stored instruction selectable from any VIM section for parallel execution with any other stored instruction associated with a different functional limit of the plurality functional execution units (Fig.1, stream processor executes 2 or 3 instructions concurrently); and a VIM load controller for separately controlling the loading of each received instruction of the plurality of instructions into a separate VIM section (Fig. 1, element 104 and RAM inputs load instructions into VIM).

10. As per claim 18, Kerr discloses claim 17 wherein each of the plurality of VIM sections has two ports allowing simultaneous read and write accesses (Fig. 1, has simultaneous loads and reads from register stack).

11. As per claim 19, Kerr discloses claim 17 wherein said line buffer temporarily stores the data packet comprising a LV2 instruction and a plurality of short instruction words SIWs, each short instruction word of the plurality of short instruction words loaded into a VIM section at an address specified in the LV2 instruction (Fig. 2A, element 202).

12. As per claim 20, Kerr discloses a method for loading VIM through a DMA controller (Fig. 2A, element 208), said method comprising: providing a VLIW memory (VIM) having a plurality of VIM sections (Fig. 1, element 101), each VIM section storing instructions corresponding to a functional execution unit of a plurality of functional execution units (Fig. 1, plurality of execution units, e.g., element 104 and 105), each stored instruction selectable from any VIM section for parallel execution with any other stored instruction associated with a different functional unit (even registers are executed in parallel with odd registers);

receiving a data packet having a plurality of instructions into a line buffer (Fig. 2A, element 202); and selectively loading each instruction of the plurality of instructions from said line buffer to each corresponding VIM section of the plurality of VIM sections by utilizing a VIM load controller (Fig. 2A, element 100 samples data from Fig. 2A, element 202 to be loaded into VIM sections).

13. As per claim 21, Kerr discloses claim 20 wherein each separate VIM section has two ports allowing simultaneous read and write accesses, and the method further comprises: separately providing each of the two parts for each separate VIM section its open address and read or write control signals (Fig. 2A, element 210).

14. As per claim 22, Kerr discloses claim 20 further comprising: temporarily storing in said line buffer a plurality of data packets comprising a LV2 instruction and a plurality of SIWs (Fig. 2A, element 202), wherein the selectively loading step loads each VIM section sequentially, for each data packet, wherein the starting address of each VIM section is determined by the addresses contained in the LV2 instruction (to load data from the line buffer, must have an address to reference where the data exists in line buffer, Fig. 2A, element 210).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to parallel processing with VLIW.

U.S. Pat. No. 6,065,106 to Deao et al.

U.S. Pat. No. 5,056,015 to Baldwin et al.

U.S. Pat. No. 6,002,880 to Slavenburg

U.S. Pat. No. 6,044,450 to Tsushima et al.

U.S. Pat. No. 6,058,474 to Baltz et al.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
06/28/2004

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100